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AMI/NRZ LINE INTERFACE FOR BASIC ACCESS ISDN IN INDOOR INFRA-RED LINKS

Indexing terms: Digital communication systems, Integrated services digital network, Decoding, Codes and coding, Circuit theory and design

An AMI/NRZ line interface applicable to basic access ISDN links for indoor infra-red communication systems is described. It provides clock extraction with negligible jitter and complies with the CCITT I.430 recommendations.

Introduction: To combine and exploit the capabilities of the ISDN with the inherent advantages of infra-red diffuse radiation,[1,2] a special interface would be needed. The task of the interface would be to adapt the AMI code used in the basic rate interface (CCITT I.430 recommendations) to the infra-red link requirements. The ISDN-to-IR link interface consists of several building blocks. We describe the first major building block: the AMI/NRZ line interface. The tasks of the AMI/NRZ line interface are

(*a*) to properly decode the incoming AMI signal into two NRZ signals and extract the data rate clock (192 kHz)

(*b*) to properly encode the received NRZ signals, i.e. those from the building blocks of the other interface, to AMI code.

To our knowledge, such a circuit that performs the above mentioned tasks for the basic rate interface has not appeared in the literature.

AMI/NRZ line interface: The operation of the circuit, which is relatively simple in construction but not so obvious in function, is explained below.

AMI/NRZ decoding section: A circuit has been developed (Fig. 1) that converts the AMI code to two NRZ signals called $Rx+$ and $Rx-$, and extracts the clock called *RxCLK* from the incoming data. Fig. 2 shows the corresponding waveforms. The conversion of AMI code to the two NRZ signals should obey the following rules:

AMI: '1'	$Rx+$: logical 1	$Rx-$: logical 1
AMI: '0+'	$Rx+$: logical 1	$Rx-$: logical 0
AMI: '0−'	$Rx+$: logical 0	$Rx-$: logical 1

The incoming AMI code is coupled through the 1 : 1 transformer to two voltage comparators U1A and U2A (LM339). The input must not exceed 4·5 V peak to peak to assure proper function of the LM339. Setting, properly, a positive and a negative threshold we obtain the two desired NRZ signals ($Rx+$, $Rx-$), each having 5·21 μs (or a multiple) pulse width. The clock recovery circuit uses a tuned LC network driven by the collector of an *npn* transistor. Clock recovery is accomplished as follows: the output data signals, $Rx+$ and $Rx-$, are fed to a dual retriggerable monostable multivibrator (74HC123), producing very short pulses, approximately 100 ns.

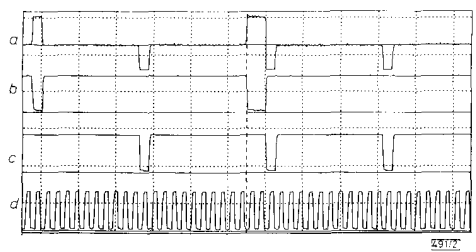

Fig. 2 *AMI-to-NRZ waveforms*
a Incoming AMI code (0·8 V/division)
b $Rx+$ (4 V/division)
c $Rx-$ (4 V/division)
d *RxCLK* (4 V/division)
Horizontal scale: 20 μs/division

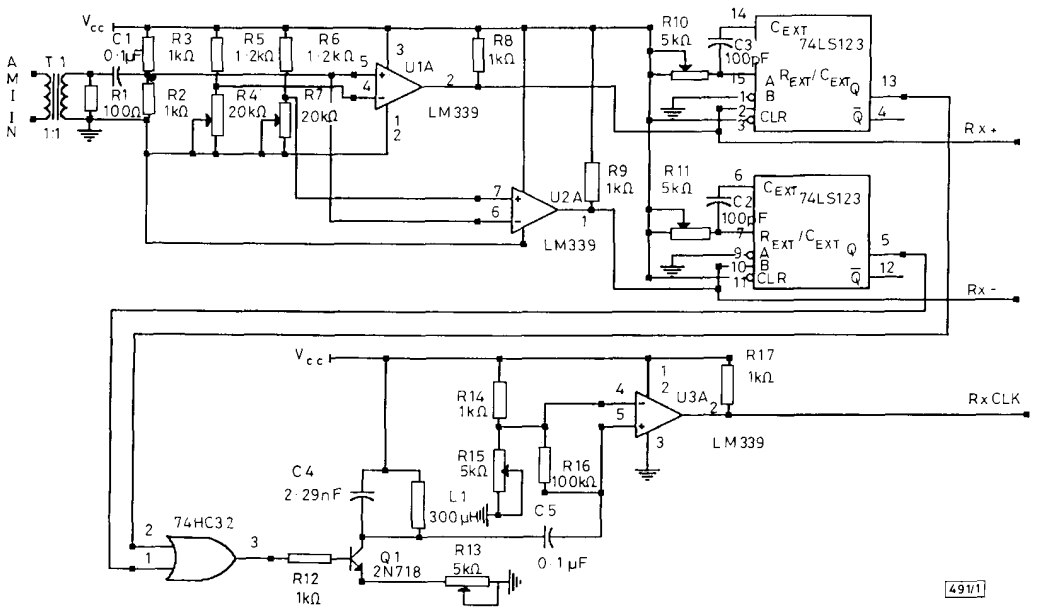

Fig. 1 *AMI-to-NRZ line interface decoding circuitry*

The reason for producing these short pulses is that the shorter the applied pulse at the base of transistor Q1 (2N718) the less the output sinewave is distorted, thus producing minimum jitter. The outputs of the 74HC123 are applied to a two-input OR gate. The created pulse pattern has a strong component at the frequency to which the LC circuit is tuned (192 kHz). This frequency is given by $1/2\pi(LC)^{1/2}$. The values of the components used are: $L = 300\,\mu$H and $C = 2{\cdot}290$ nF. The pulse pattern drives an *npn* output transistor Q1. Each time a pulse is applied to the base of transistor Q1, this transistor turns on and energy is stored in inductor L and capacitor C. When no pulse exists, Q1 turns off and the stored energy in the LC tank discharges producing at the collector of transistor Q1 a sinewave oscillating at 192 kHz. The recovered sinewave from this tuned circuit is then fed into another voltage comparator (U3A) which converts the sinusoidal waveform into a rectangular pattern (*RxCLK*). The produced rectangular clock pattern exhibits very low jitter (40 ns), which is much less than the recommended by the I.430 recommendation (−7%–+7% of the 5·21 μs bit period).

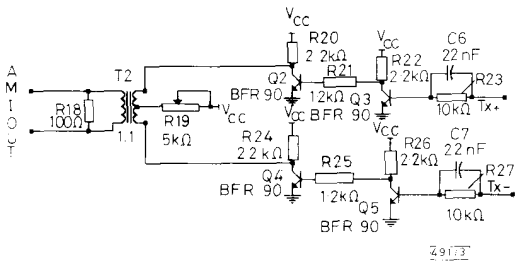

Fig. 3 *NRZ-to-AMI line interface encoding circuitry*

NRZ/AMI encoding section: The NRZ to AMI encoding section, shown in Fig. 3, converts the digital data called $Tx+$ and $Tx-$ to an AMI code in accordance with the CCITT I.430 recommendation. $Tx+$ and $Tx-$ are two NRZ signals with the same pulse width, 5·21 μs, as occurs with $Rx+$ and $Rx-$ and already synchronised with *RxCLK*). Fig. 4 shows the corresponding waveforms for the circuit of Fig. 3.

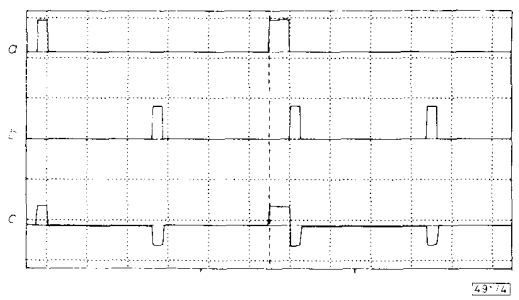

Fig. 4 *NRZ-to-AMI waveforms*
a $Tx+$ (6 V/division)
b $Tx-$ (6 V/division)
c Output AMI code (1·5 V/division)
Horizontal scale: 20 μs/division

Explanation of results: The two circuits were breadboarded and tested and the waveforms obtained are shown in Figs. 2 and 4 as mentioned previously. The output NRZ signals $Rx+$, $Rx-$ and the extracted clock of 192 kHz, *RxCLK*, were obtained. The pulse width of the two NRZ signals was 5·21 μs and the extracted clock jitter approximately 40 ns. This means that the extracted clock is well defined and capable of synchronising the rest of the interface.

A comparison between the input AMI signal and the output AMI shows that the peak to peak voltages are exactly the same. The comparison also shows that the total phase deviation (TPD) of input to output is negligible (100 ns measured) as the I.430 recommendation permits a TPD of −7% to +15% for a 5·21 μs bit period.

Closing remarks: This paper describes the development of special interface AMI/NRZ circuits as part of an ISDN-to-IR connection link. The developed circuits were successfully tested using the TP3500 ISDN evaluation system by National Semiconductor Corporation which consists of two ISDN basic rate interface boards. The tests included voice and data transmission.

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DESIGN AND TEST OF NOVEL INTEGRATE AND DUMP FILTER (I&D) FOR OPTICAL Gbit/s SYSTEM APPLICATIONS

Indexing terms: Filters, Digital communication systems, Optical communications

An innovative integrated and dump circuit (I&D) attractive for Gbit/s applications is presented. The new circuit avoids the dumping signal. Initial tests indicate that the I&D improves the receiver sensitivity of 1 Gbit/s baseband and optical DPSK systems.

Introduction: Integrated and dump circuits (I&Ds) are of general interest for all communication systems, where they are applied e.g. as matched filters in baseband systems or as subcomponents in correlation receivers in RF systems.[1] Applications of I&Ds in high speed optical transmission systems have been published.[2–4]

The conventional circuit suffers from several drawbacks related to the dumping process, the most crucial point in high speed circuits.

(i) A generator for the dumping pulse with a bandwidth several octaves higher than that of the other electronic circuit is needed:

(ii) Owing to the finite duration time T_D of the dumping pulse the effective integration time in a time slot $(k-1)\,.\,T < t \leq k\,.\,T$ is reduced to $T - T_D$, where T is the bit period and k is an integer. ($T - T_D$ equal to 75% of T is achieved in Reference 3). This leads to loss of receiver sensitivity and in Reference 3 better performance was obtained using a conventional baseband noise filter.

(iii) Parasitic capacitors of the transistors involved have to be used as the integrating elements.[2,3] They also cause feedthrough of the high power dumping pulses to other circuit elements.

Innovative I&D concept: In an I&D the integrated signal is sampled at the end of each time slot at $t = k\,.\,T$ (see Fig. 1*a*). The signal shape and the amplitude during the integration time $(k-1)\,.\,T < t \leq kT$ are of no concern. The only prerequisite is that the signal of the preceding time slot $(k-2)\,.\,T < t \leq (k-1)\,.\,T$ and those before have no influence at the time of sampling $t = k\,.\,T$. In the conventional setup this is achieved by the dumping pulse being immediately applied when the sampling has taken place. The dumping also prevents the integrator from being saturated by a sequence of